Radiation Hardened 30V 16-Channel Analog Multiplexer

ISL71840SEH

The ISL71840SEH is a radiation hardened, 16-channel high ESD protected multiplexer that is fabricated using Intersil's proprietary P6SOI (Silicon On Insulator) process technology to mitigate single-event effects and total ionizing dose. It operates with a dual supply voltage ranging from ±10.8V to ±16.5V. It has a 4-bit address plus an enable pin that can be driven with adjustable logic thresholds to conveniently select 1 of 16 available channels. An inactive channel is separated from an active channel by a high impedance, which inhibits any interaction between them.

The ISL71840SEH's low r_{ON} allows for improved signal integrity and reduced power losses. The ISL71840SEH is also designed for cold sparing making it excellent for high reliability applications that have redundancy requirements. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without loading signal sources. The ISL71840SEH also incorporates input analog overvoltage protection, which will disable the switch to protect downstream devices.

The ISL71840SEH is available in a 28 Ld CDFP or die form and operates across the extended temperature range of -55°C to +125°C.

There is also a 32-channel version available offered in a 48 Ld CQFP, please refer to the ISL71841SEH datasheet for more information. For a list of differences please refer to Table 1 on page 3.

Related Literature

- UG028, "ISL71840SEHEV1Z Evaluation Board User Guide"
- TR004, "Single Event Effects (SEE) Testing of the ISL71840SEH 16:1 30V Mux"
- TR010, "Total Dose Testing of the ISL71840SEH 16-Channel Analog Multiplexer"

Features

- DLA SMD# 5962-15219
- Fabricated using P6SOI process technology
  - Provides latch-up immunity
- ESD protection 8kV (HBM)
- Rail-to-rail operation
- Overvoltage protection
- Low r_{ON} . . . . . <500Ω (typical)
- Flexible split rail operation
  - Positive supply above GND (V^+) . . . . . +10.8V to +16.5V
  - Negative supply below GND (V^-) . . . . . -10.8V to -16.5V
- Adjustable logic threshold control with VREF Pin
- Cold sparing capable (from ground). . . . . ±25V
- Analog overvoltage range (from ground). . . . . ±35V
- Off switch leakage . . . . . 100nA (max)
- Transition times (t_R, t_F) . . . . . 500ns (typ)
- Break-before-make switching
- Grounded metal lid (internally connected)
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . 100krad(Si) (see Note)
  - SEB LET_{TH} . . . . . 86.4 MeV•cm^2/mg

NOTE: Product capability established by initial characterization. All subsequent lots are assurance tested to 50krad (0.01rad(Si)/s) wafer-by-wafer.

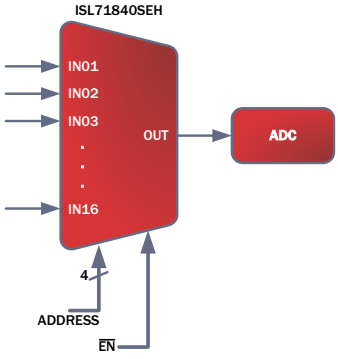


FIGURE 1. TYPICAL APPLICATION

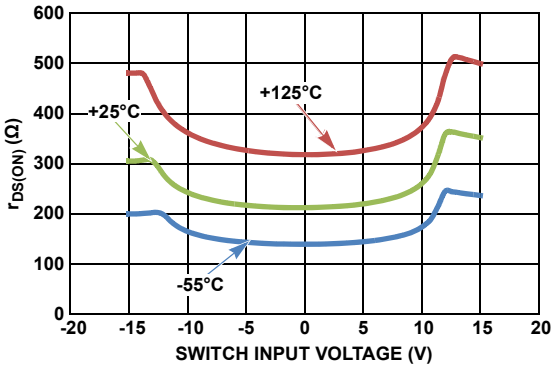


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY ACROSS SWITCH INPUT COMMON MODE VOLTAGE AT +25°C

Table of Contents

Ordering Information

ORDERING/SMD NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R1521901VXC	ISL71840SEHVF	-55 to +125	28 LD CDFP	K28.A
ISL71840SEHF/PROTO	ISL71840SEHF/PROTO	-55 to +125	28 LD CDFP	K28.A
5962R1521901V9A	ISL71840SEHVX	-55 to +125	DIE	
ISL71840SEHX/SAMPLE	ISL71840SEHX/SAMPLE	-55 to +125	DIE	
ISL71840SEHEV1Z	Evaluation Board			

NOTES:

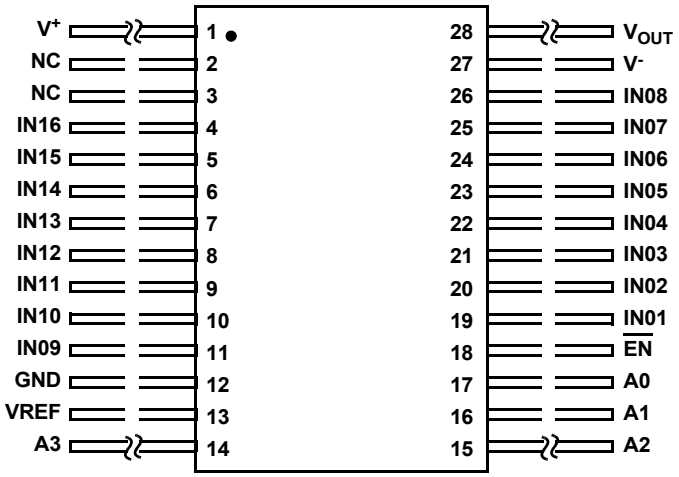
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.

TABLE 1. TABLE OF DIFFERENCES

SPEC	ISL71840SEH	ISL71841SEH
Number of Channels	16	32
Supply Current (I+/I-)	350µA (Max)	400µA (Max)
Output Leakage (+125°C)	60nA (Max)	120nA (Max)

Pin Configuration

ISL71840SEH
(28 LD CDFP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{OUT}	28	Output for multiplexer
V^+	1	Positive power supply
V^-	27	Negative power supply
NC	2, 3	Not electrically connected
INx	4, 5, 6, 7, 8, 9, 10, 11, 19, 20, 21, 22, 23, 24, 25, 26	Input for multiplexer
Ax	14, 15, 16, 17	Address lines for multiplexer
$\overline{EN}$	18	Enable control for multiplexer (active low)
VREF	13	Reference voltage used to set logic thresholds
GND	12	Ground
LID	N/A	Package Lid is internally connected to GND (Pin 12)

Absolute Maximum Ratings

Positive Supply Voltage above GND (V^+) (Note 5) . . . . . +20V
Negative Supply Voltage below GND (V^-) (Note 5 . . . . . -20V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 5) 40V
Maximum Current Through Selected Switch. 10mA
Analog Input Voltage (INx)
From GND (Note 5) . . . . . ±35V
Digital Input Voltage Range ($\overline{EN}$, Ax) . . . . . GND to V^+
VREF to GND (Note 5) 16.5V
ESD Tolerance
Human Body Model (Tested per MIL-STD-883 TM 3015) 8kV
Charged Device Model (Tested per JESD22-C101D) 250V
Machine Model (Tested per JESD22-A115-A) 250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld CDFP (Notes 3, 4)	48	4

Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Positive Supply Voltage Above GND (V^+) . . . . . +10.8V to +16.5V
Negative Supply Voltage Below GND (V^-) . . . . . -10.8V to -16.5V
Supply Voltage Differential (V^+ to V^-) . . . . . 21.6V to 33V
VREF to GND . . . . . 4.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.
5. Tested in a heavy ion environment at LET = 86.3 MeV • cm^2/mg at +125°C.

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_S	Analog Input Signal Range		V^-	-	V^+	V
r_{ON}	Channel ON-resistance	V± = ±15.0V, ±16.5V I_{OUT} = -1mA, V_{IN} = +5V, -5V	**-**	-	**500**	Ω
		V± = ±15.0V, ±16.5V I_{OUT} = -1mA, V_{IN} = V^+, V^-	**-**	-	**700**	Ω
Δr_{ON}	r_{ON} Match Between Channels	V_{IN} = +5V, -5V; I_{OUT} = -1mA	-	10	**20**	Ω
$R_{FLAT(ON)}$	ON-resistance Flatness	V_{IN} = +5V, -5V	**-**	-	**25**	Ω
$I_{S(OFF)}$	Switch Off Leakage	V_{IN} = V^+ - 5V, V± = ±16.5V, All unused inputs are tied to V^- + 5V	**-10**	-	**10**	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V^- + 5V, V± = ±16.5V All other inputs = V^+ - 5V T_A = +25°C	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-100	-	100	nA
$I_{S(OFF)\ POWER\ OFF}$	Switch Off Leakage with Device Powered Off	V_{IN} = +25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA

Electrical Specifications (±15V) V^+ = 15V, V^- = -15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$I_{S(OFF)}$ POWER OFF	Switch Off Leakage with Device Powered Off	V_{IN} = +25V, $V_{\overline{EN}}/V_A/V_{REF}$ = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, $V_{\overline{EN}}/V_A/V_{REF}$ = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA
$I_{S(ON)}$ OVERVOLT	Switch On Leakage Current Into the Source (overvoltage)	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-500	-	500	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-500	-	500	nA
$I_{S(OFF)}$ OVERVOLT	Switch Off Leakage Current Into the Source (overvoltage)	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-750	-	750	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-750	-	750	nA
$I_{D(OFF)}$	Switch Off Leakage	V_{OUT} = V^+ - 5V, All inputs = V^- + 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	0	-	60	nA
		Post radiation	-80	-	80	nA
		V_{OUT} = V^- + 5V, All inputs = V^+ - 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-60	-	0	nA
		Post radiation	-80	-	80	nA

Electrical Specifications (±15V) V^+ = 15V, V^- = -15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$I_{D(OFF)\ OVERVOLT}$	Switch Off Leakage Current Into the Drain (overvoltage)	V_{OUT} = 0V, V_{IN} = +35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA
		V_{OUT} = 0V, V_{IN} = -35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA
$I_{D(ON)}$	Switch On Leakage Current Into the Source/Drain	V_{IN} = V_{OUT} = V^+ - 5V, T_A = +25°C, -55°C All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	0	-	60	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V_{OUT} = V^- + 5V, T_A = +25°C, -55°C All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-60	-	0	nA
		Post radiation	-100	-	100	nA
$V_{AH/L}$, $V_{ENH/L}$	Logic Input High/Low Voltage	V_{REF} = 5.0V	**1.2**	-	**1.6**	V
I_{AH}, I_{ENH}	Input Current with V_{AH}, V_{ENH}	V_A = $V_{\overline{EN}}$ = 4.0V V^+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
I_{AL}, I_{ENL}	Input Current with V_{AL}, V_{ENL}	V_A = $V_{\overline{EN}}$ = 0.8V V^+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
I+	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**350**	µA
I-	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**-350**	-	-	µA
I+	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	-	-	**350**	µA
I-	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	**-350**	-	-	µA
I_{REF}	Supply Current Into V_{REF}	V_{REF} = 5.5V, V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**35**	µA
DYNAMIC						
t_{ALH}	Transition Time	Figures 4, 5	-	0.5	**800**	ns
t_{AHL}	Transition Time	Figures 4, 5	-	0.5	**800**	ns
t_{BBM}	Break-before-make Delay	Figures 8, 9	**5**	50	**200**	ns
		Post radiation	**5**	-	**400**	ns
t_{ENABLE}	Enable Turn-on Time	Figures 6, 7	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
$t_{DISABLE}$	Disable Turn-off Time	Figures 6, 7	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
V_{CTE}	Charge Injection	C_L = 100pF, V_{IN} = 0V, (Figure 6)	-	2	5	pC
V_{ISO}	OFF Isolation	$V_{\overline{EN}}$ = 4V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	75	-	-	dB
V_{CT}	Crosstalk	$V_{\overline{EN}}$ = 0.8V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	47	-	-	dB
C_A	Digital Input Capacitance	f = 1MHz, V^+ = V^- = 0V	-	-	**7**	pF
$C_{IN(OFF)}$	Input Capacitance	f = 1MHz, V^+ = V^- = 0V	-	-	**5**	pF
$C_{OUT(OFF)}$	Output Capacitance	f = 1MHz, V^+ = V^- = 0V	-	-	**50**	pF

Electrical Specifications (±12V) V^+ = 12V, V^- = -12V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A = +25°C, unless otherwise noted.

Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_S	Analog Input Signal Range		V^-		V^+	V
r_{ON}	Channel ON-resistance	V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = +5V, -5V	**-**	-	**500**	Ω
		V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = V^+, V^-	**-**	-	**700**	Ω
Δr_{ON}	r_{ON} Match Between Channels	V_{IN} = +5V, -5V; I_{OUT} = -1mA	-	10	**20**	Ω
$R_{FLAT(ON)}$	ON-resistance Flatness	V_{IN} = +5V, -5V, V± = ±13.2V	**-**	-	**25**	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V T_A = +25°C, -55°C, +125°C	-	-	30	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, post radiation	**-**	-	**40**	Ω
I+	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-**	**-**	**350**	µA
I-	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-350**	**-**	**-**	µA
I+	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	**-**	**-**	**350**	µA
I-	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	**-350**	**-**	**-**	µA
I_{REF}	Supply Current Into V_{REF}	V_{REF} = 5.5V, V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-**	-	**35**	µA
DYNAMIC						
t_{ALH}	Transition Time	Figures 4, 5	**-**	0.5	**800**	ns
t_{AHL}	Transition Time	Figures 4, 5	**-**	0.5	**800**	ns
t_{BBM}	Break-before-make Delay	Figures 8, 9	**5**	50	**200**	ns
		Post radiation	**-**	-	**400**	ns
t_{ENABLE}	Enable Turn-on Time	Figures 6, 7	**-**	0.5	**600**	ns
		Post radiation	**-**	-	**800**	ns
$t_{DISABLE}$	Disable Turn-off Time	Figures 6, 7	**-**	0.5	**600**	ns
		Post radiation	**-**	-	**800**	ns

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 2. TRUTH

A3	A2	A1	A0	$\overline{EN}$	"ON" Channel
X	X	X	X	1	None
0	0	0	0	0	1
0	0	0	1	0	2
0	0	1	0	0	3
0	0	1	1	0	4
0	1	0	0	0	5
0	1	0	1	0	6
0	1	1	0	0	7
0	1	1	1	0	8
1	0	0	0	0	9
1	0	0	1	0	10
1	0	1	0	0	11
1	0	1	1	0	12
1	1	0	0	0	13
1	1	0	1	0	14
1	1	1	0	0	15
1	1	1	1	0	16

NOTE:

7. Don't care, "1" = Logic High, "0" = Logic Low.

Block Diagram

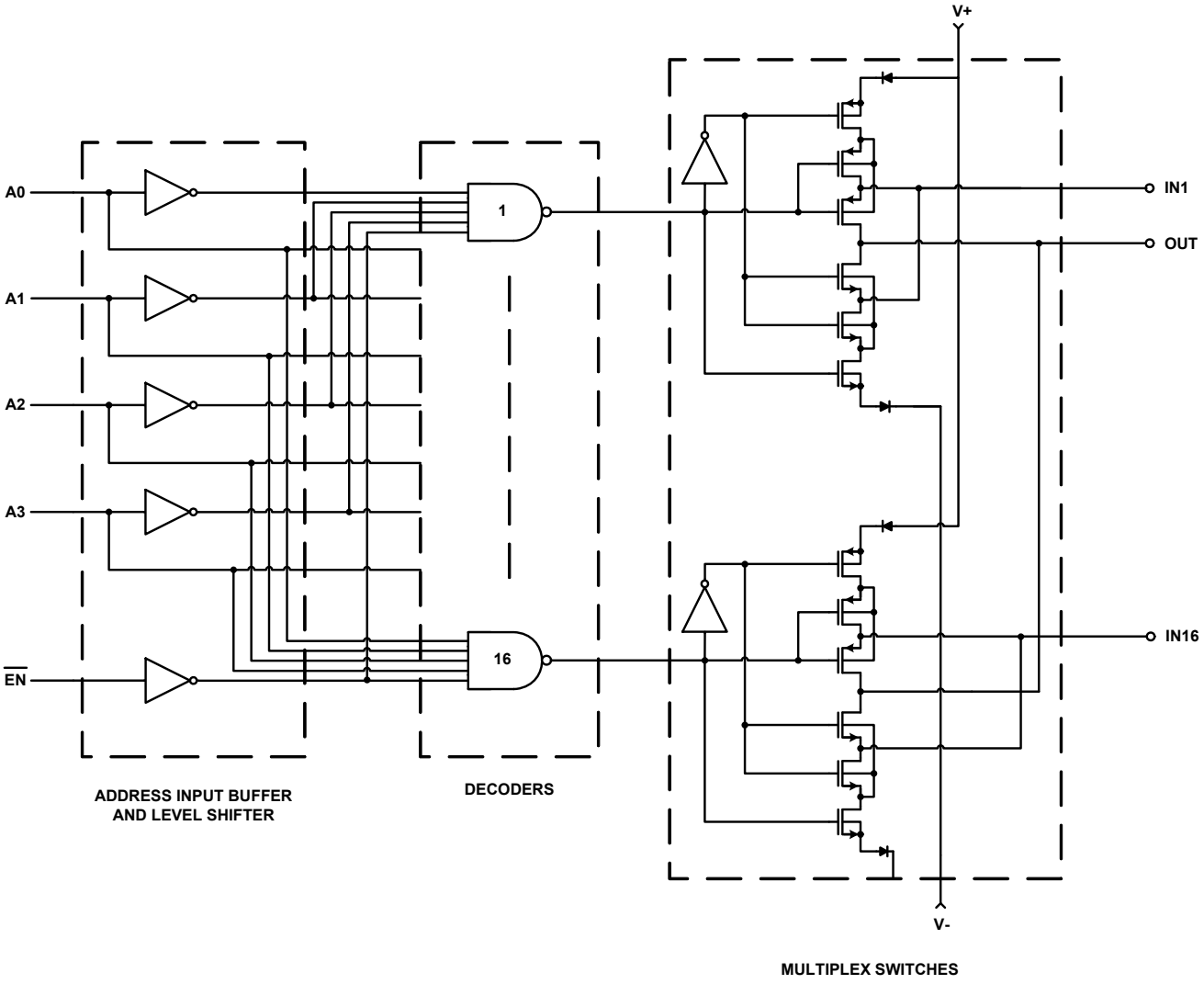


FIGURE 3. BLOCK DIAGRAM

Timing Diagrams

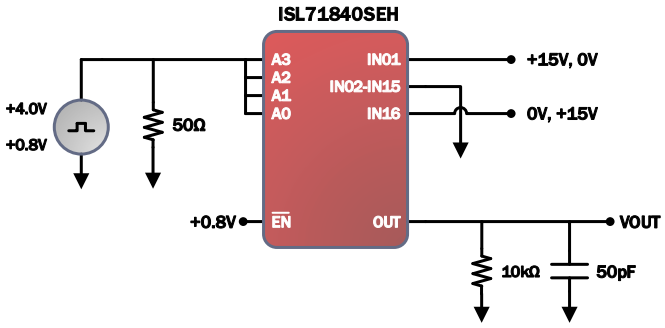


FIGURE 4. ADDRESS TIME TO OUTPUT TEST CIRCUIT

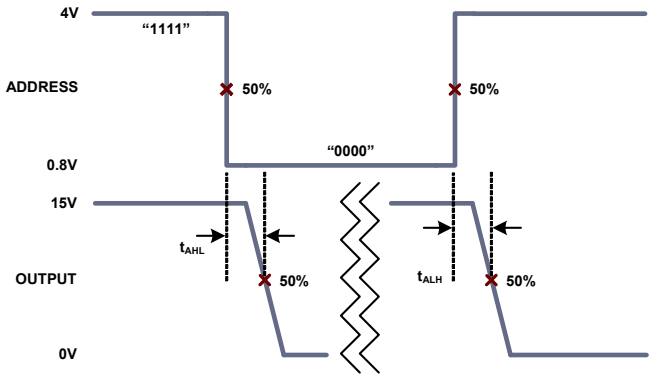


FIGURE 5. ADDRESS TIME TO OUTPUT DIAGRAM

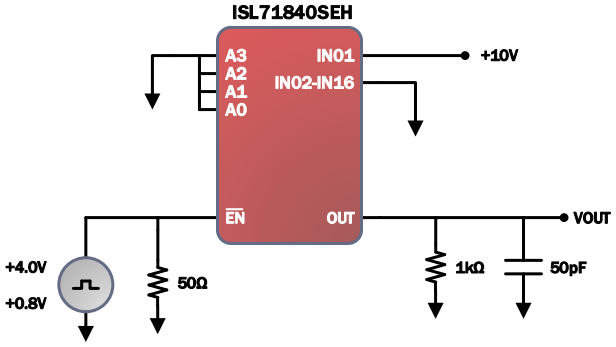


FIGURE 6. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

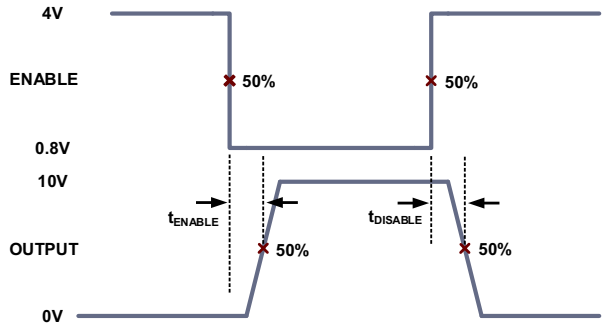


FIGURE 7. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

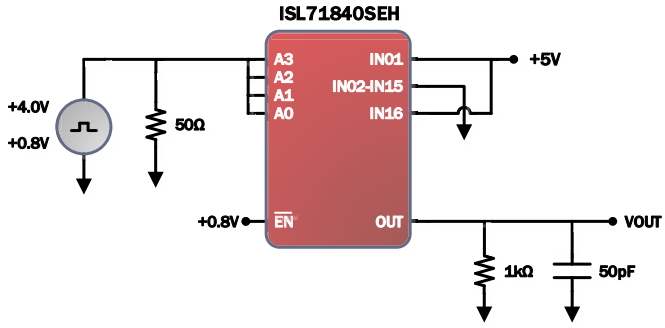


FIGURE 8. BREAK-BEFORE-MAKE TEST CIRCUIT

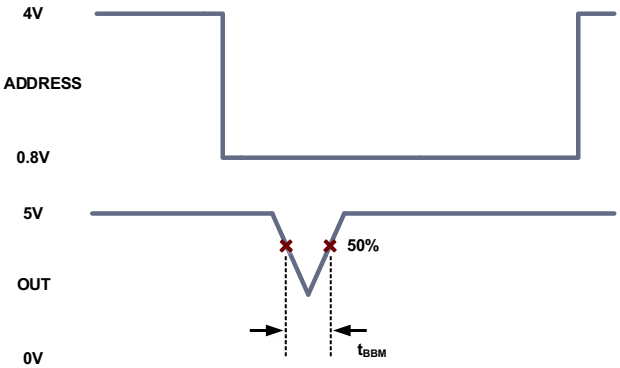


FIGURE 9. BREAK-BEFORE-MAKE DIAGRAM

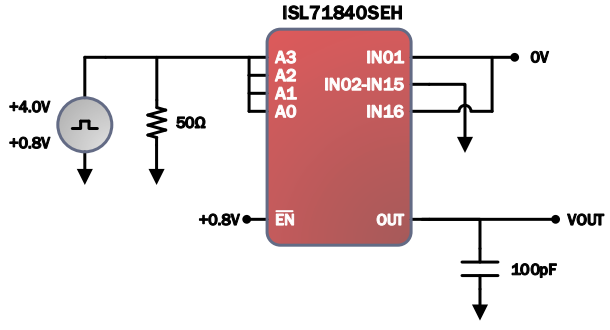


FIGURE 10. CHARGE INJECTION TEST CIRCUIT

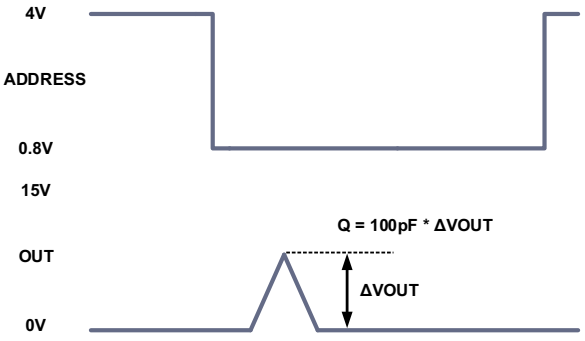


FIGURE 11. CHARGE INJECTION DIAGRAM

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified.

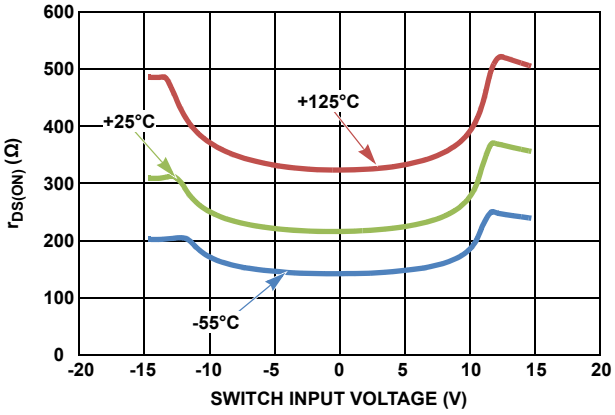


FIGURE 12. $r_{DS(ON)}$ vs VCM (V± = 14.5V)

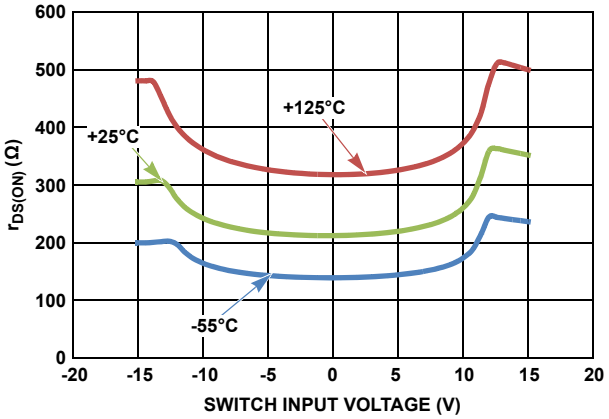


FIGURE 13. $r_{DS(ON)}$ vs VCM (V± = 15.0V)

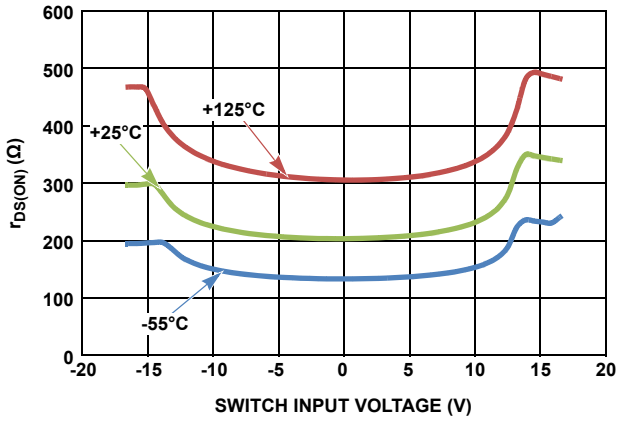


FIGURE 14. $r_{DS(ON)}$ vs VCM (V± = 16.5V)

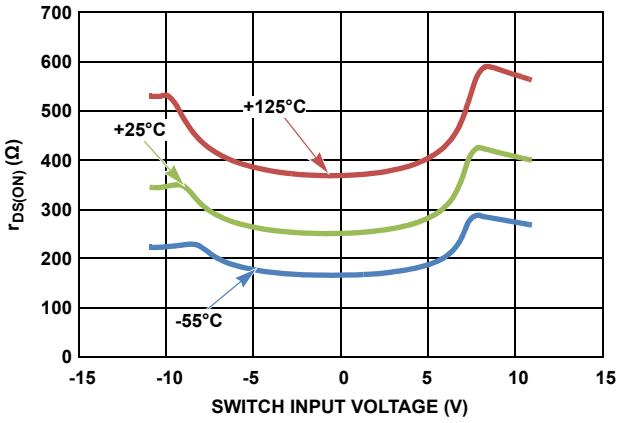


FIGURE 15. $r_{DS(ON)}$ vs VCM (V± = 10.8V)

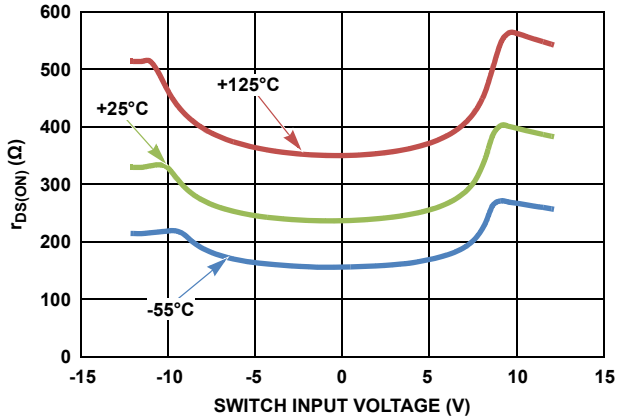


FIGURE 16. $r_{DS(ON)}$ vs VCM (V± = 12.0V)

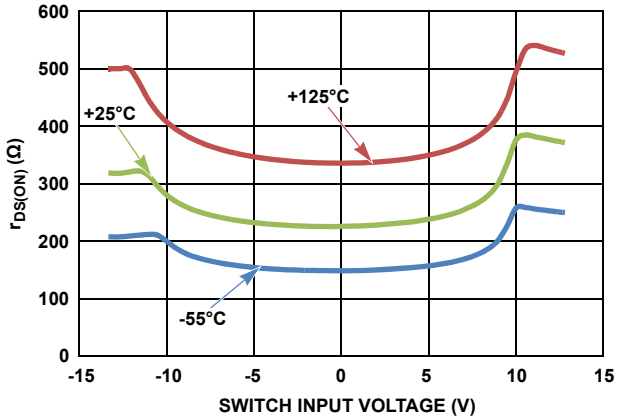


FIGURE 17. $r_{DS(ON)}$ vs VCM (V± = 13.2V)

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

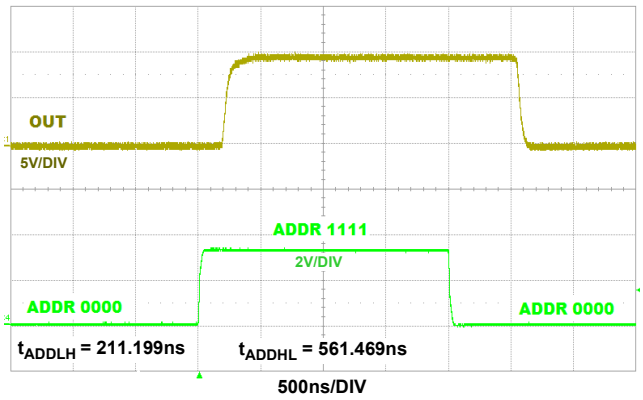


FIGURE 18. TYPICAL ADDRESS TO OUTPUT DELAY (V± = ±15V, +25°C)

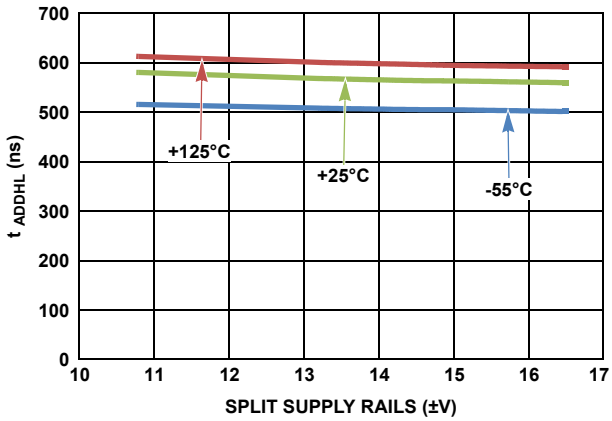


FIGURE 19. ADDRESS TO OUTPUT DELAY (HIGH-TO-LOW)

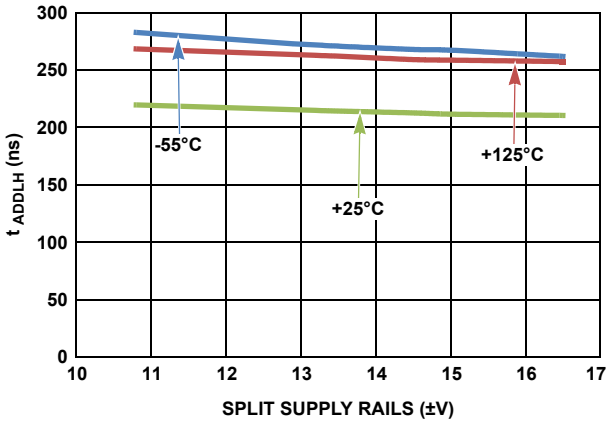


FIGURE 20. ADDRESS TO OUTPUT DELAY (LOW-TO-HIGH)

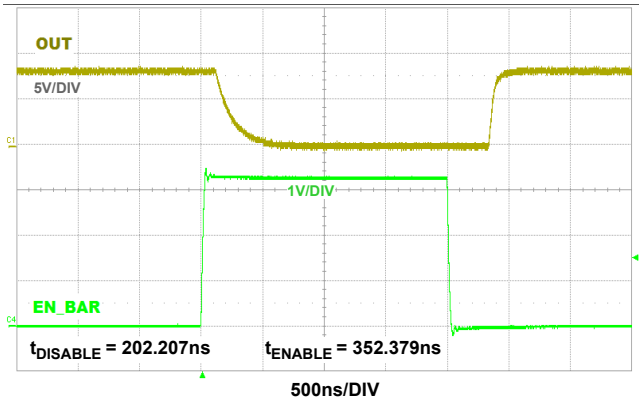


FIGURE 21. TYPICAL ENABLE TO OUTPUT DELAY (V± = ±15V, +25°C)

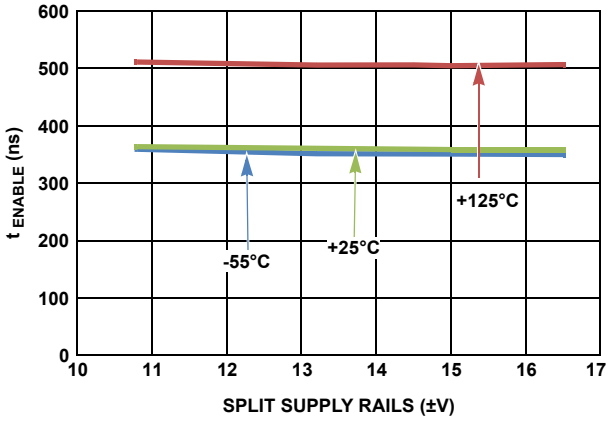


FIGURE 22. ENABLE TO OUTPUT DELAY (LOW-TO-HIGH)

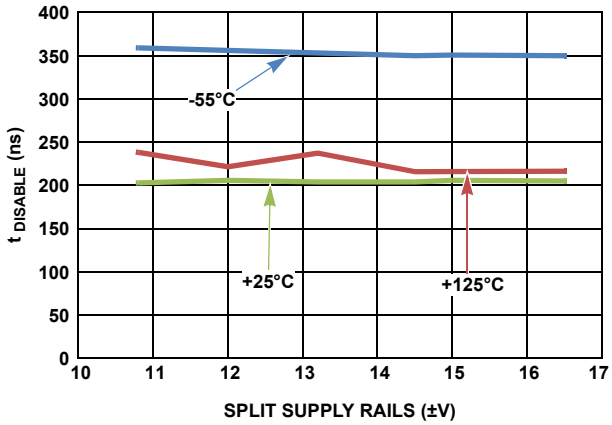


FIGURE 23. DISABLE TO OUTPUT DELAY (LOW-TO-HIGH)

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

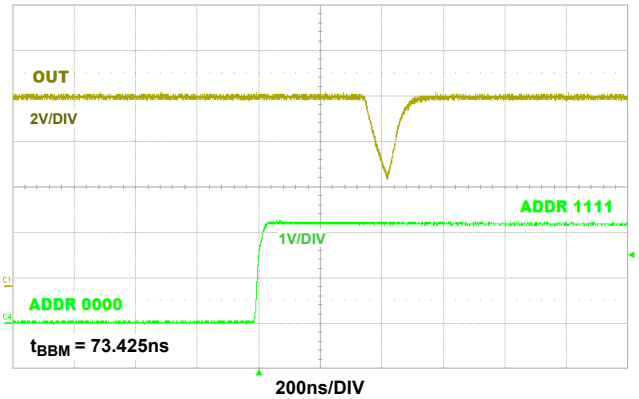


FIGURE 24. TYPICAL BREAK BEFORE MAKE DELAY (V± = 15V, +25°C)

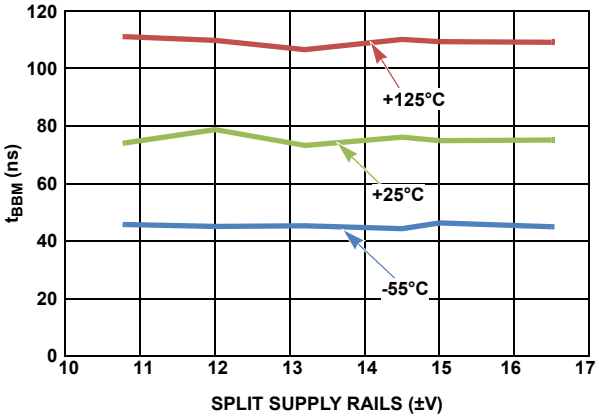


FIGURE 25. BREAK-BEFORE-MAKE DELAY

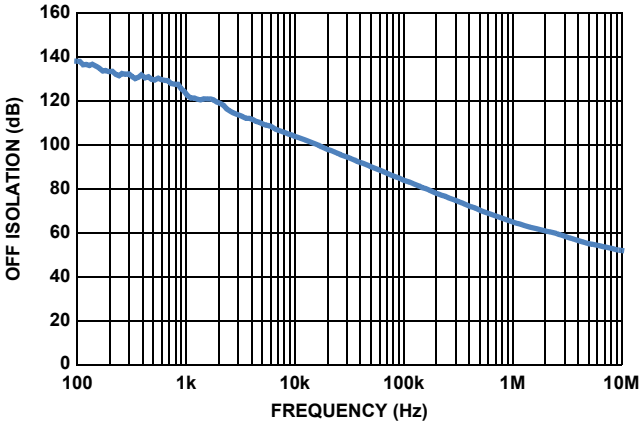


FIGURE 26. OFF ISOLATION (V± = ±15V, R_L = 1kΩ, +25°C)

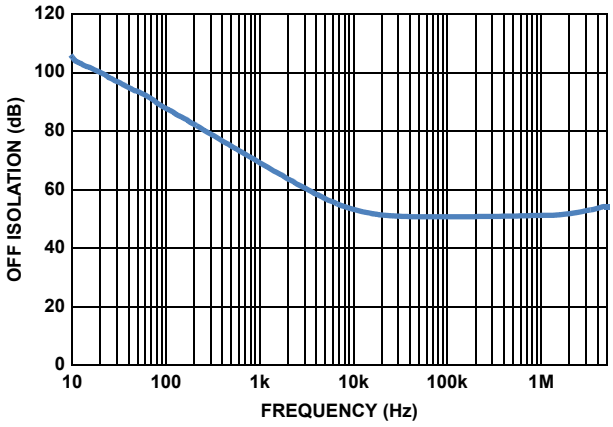


FIGURE 27. OFF ISOLATION (V± = ±15V, R_L = OPEN, +25°C)

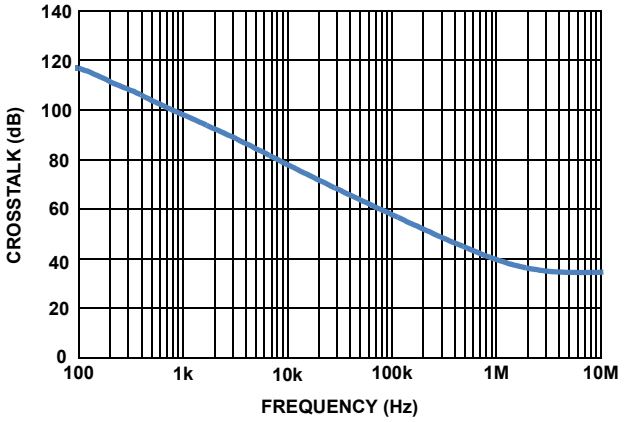


FIGURE 28. CROSSTALK (V± = ±15V, R_L = 1kΩ, +25°C)

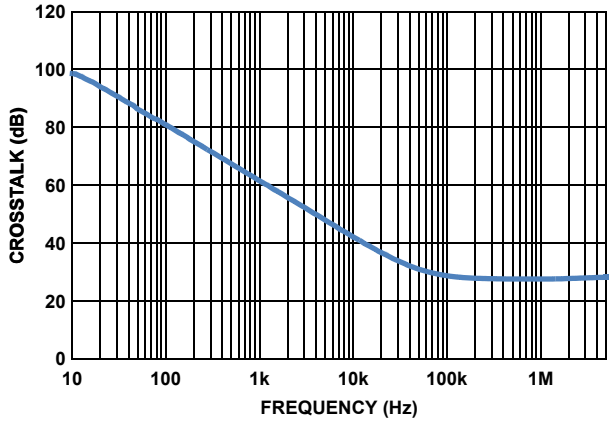


FIGURE 29. CROSSTALK (V± = ±15V, R_L = OPEN, +25°C)

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

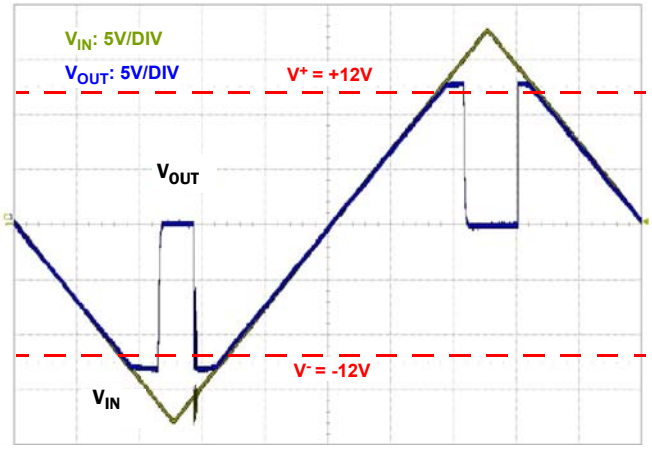


FIGURE 30. OVER/UNDERVOLTAGE PROTECTION (+25°C)

Post High Dose Rate Radiation Characteristics ($V_S = \pm15V$)

Unless otherwise specified, $V_S = \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

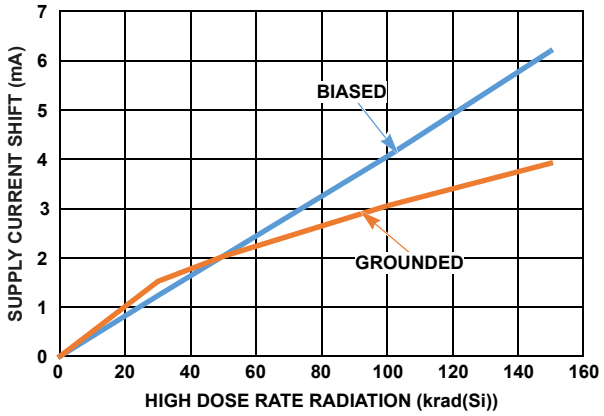


FIGURE 31. ICC SUPPLY CURRENT SHIFT vs HDR RADIATION

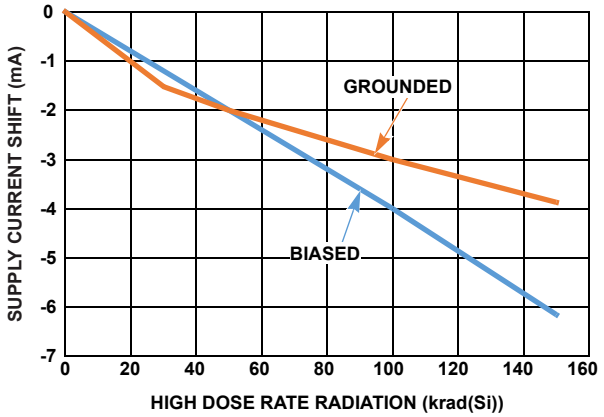


FIGURE 32. IEE SUPPLY CURRENT SHIFT vs HDR RADIATION

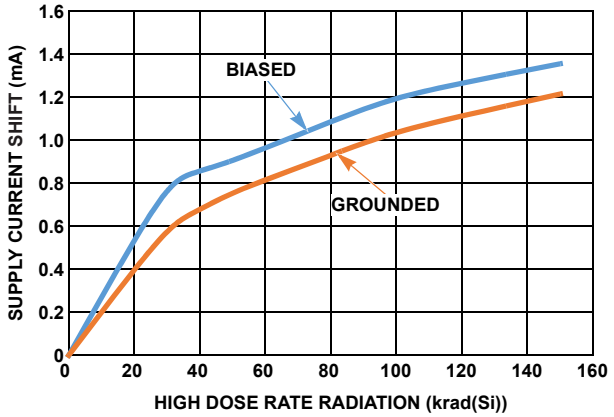


FIGURE 33. I_{REF} SUPPLY CURRENT SHIFT vs HDR RADIATION

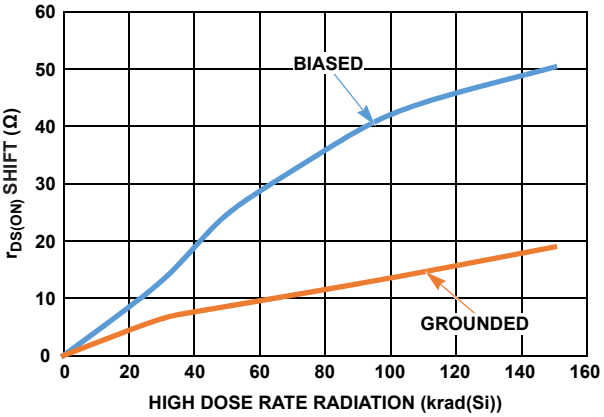


FIGURE 34. $r_{DS(ON)}$ SHIFT ($V_{IN} = V^+$) vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±15V) Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

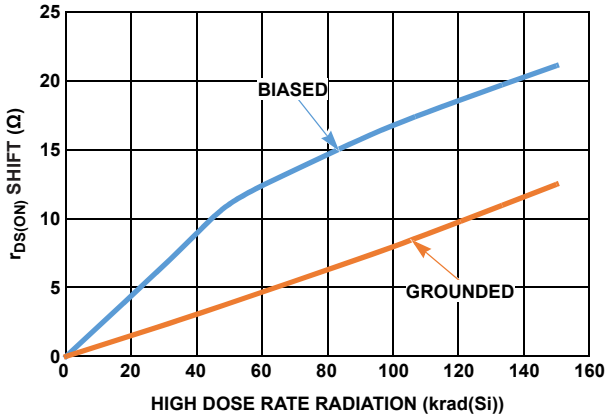


FIGURE 35. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs HDR RADIATION

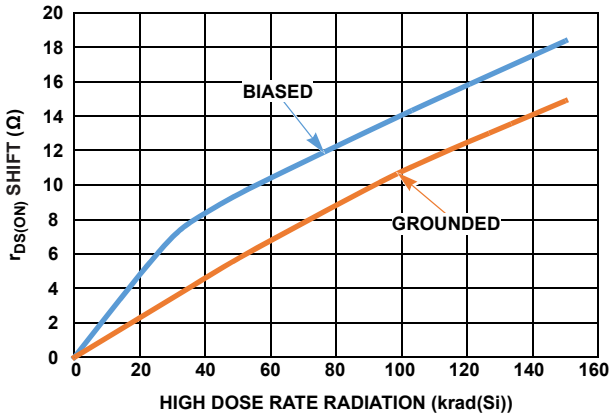


FIGURE 36. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs HDR RADIATION

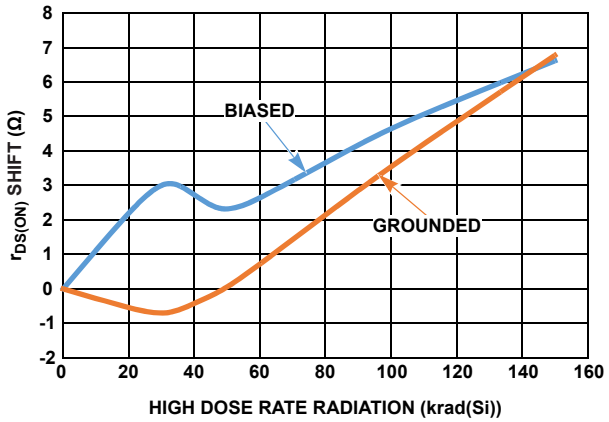


FIGURE 37. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs HDR RADIATION

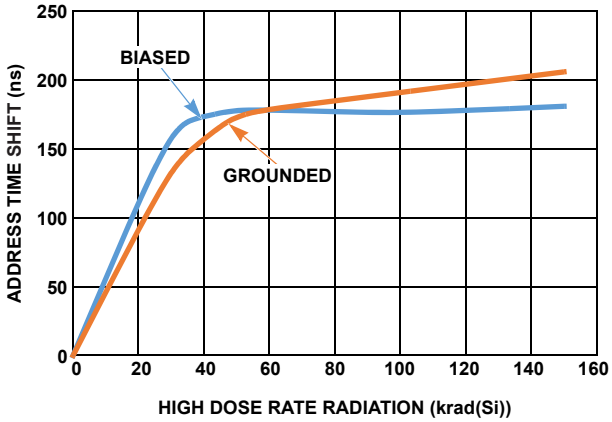


FIGURE 38. t_{ADD} SHIFT (LOW-TO-HIGH) vs HDR RADIATION

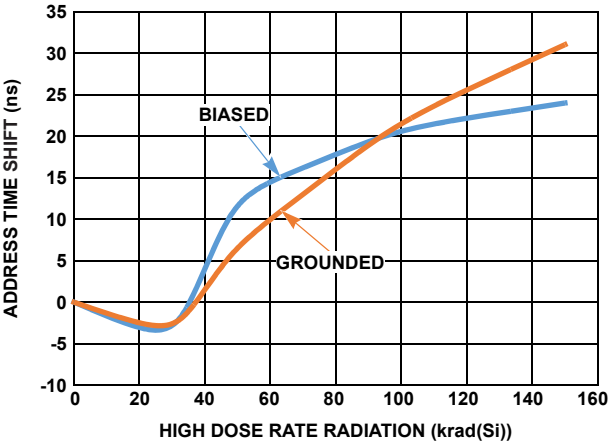


FIGURE 39. t_{ADD} SHIFT (HIGH-TO-LOW) vs HDR RADIATION

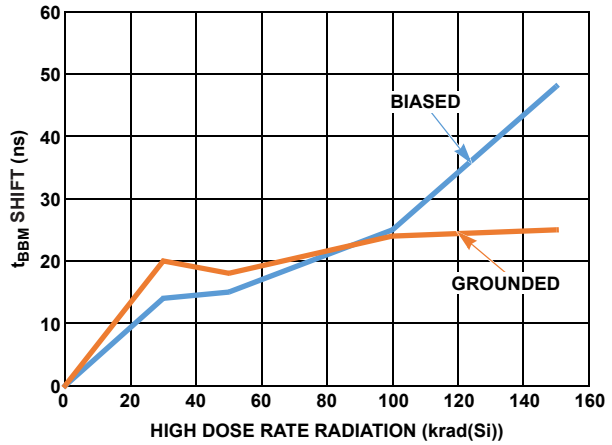


FIGURE 40. t_{BBM} SHIFT vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±15V) Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

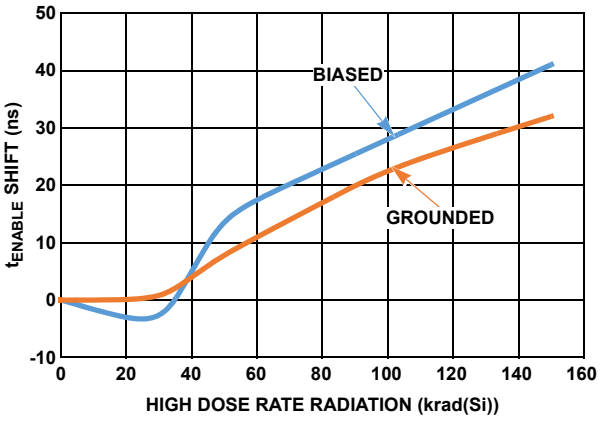


FIGURE 41. t_{ENABLE} SHIFT vs HDR RADIATION

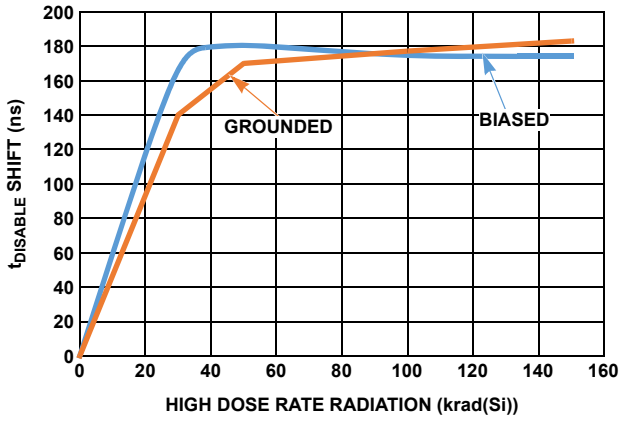


FIGURE 42. $t_{DISABLE}$ SHIFT vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±12V) Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

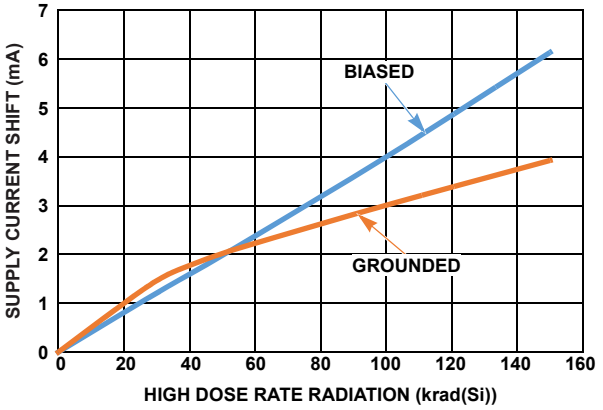


FIGURE 43. ICC SUPPLY CURRENT SHIFT vs HDR RADIATION

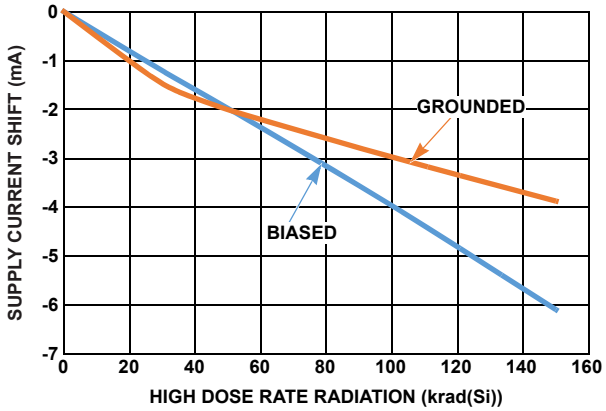


FIGURE 44. IEE SUPPLY CURRENT SHIFT vs HDR RADIATION

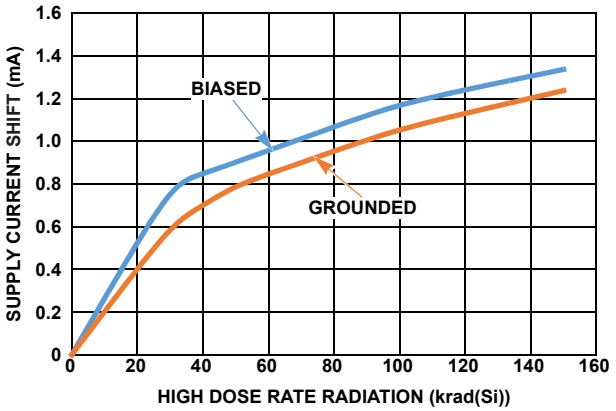


FIGURE 45. I_{REF} SUPPLY CURRENT SHIFT vs HDR RADIATION

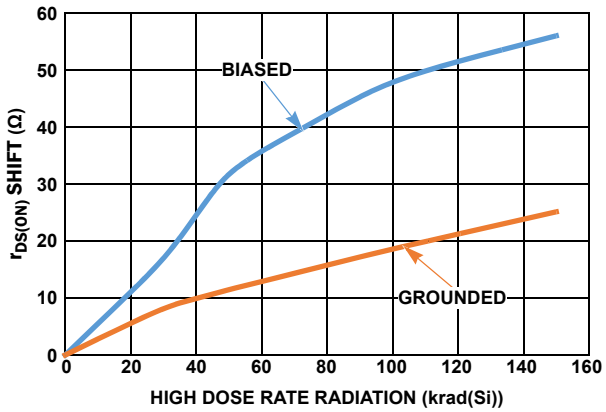


FIGURE 46. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

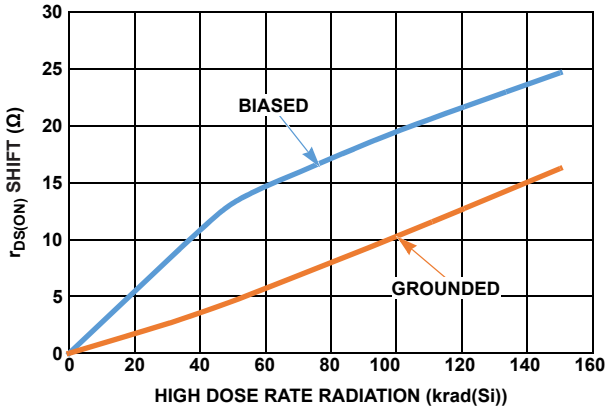


FIGURE 47. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs HDR RADIATION

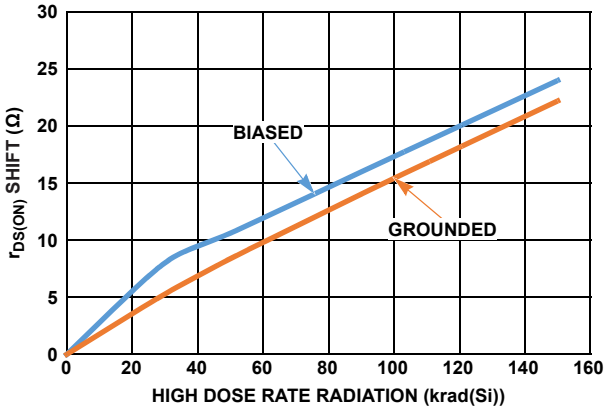


FIGURE 48. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs HDR RADIATION

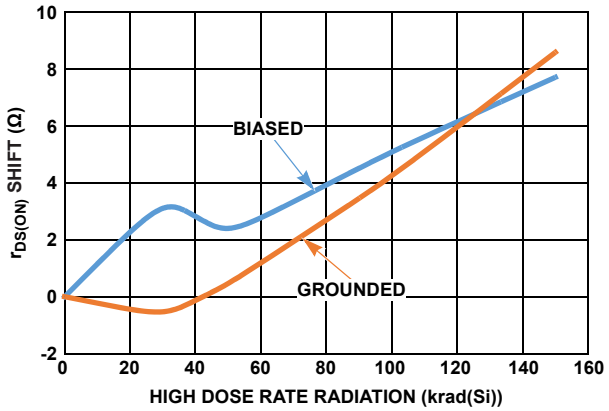


FIGURE 49. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs HDR RADIATION

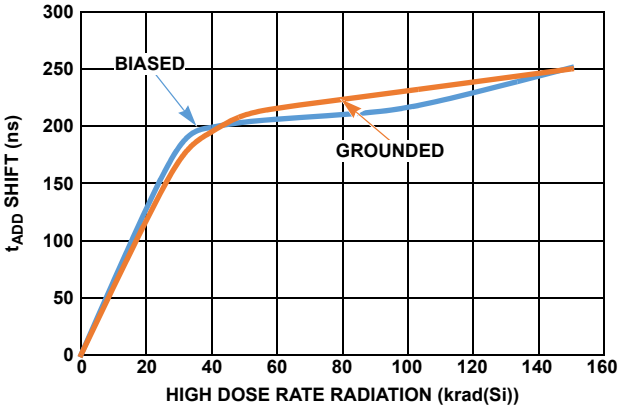


FIGURE 50. t_{ADD} SHIFT (LOW-TO-HIGH) vs HDR RADIATION

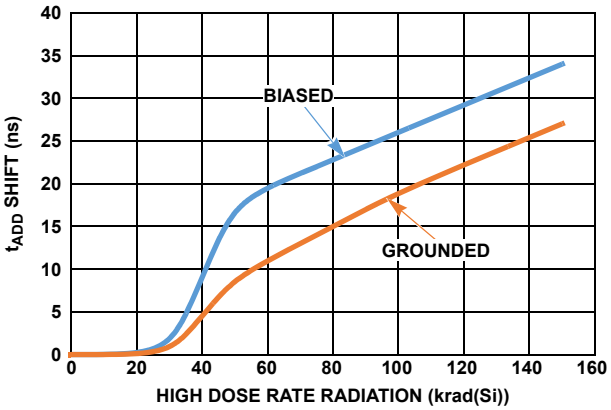


FIGURE 51. t_{ADD} SHIFT (HIGH-TO-LOW) vs HDR RADIATION

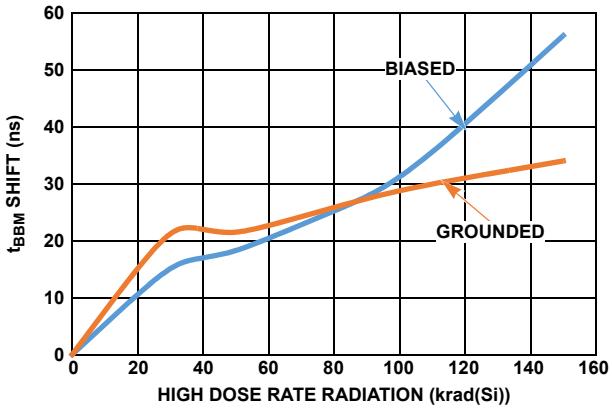


FIGURE 52. t_{BBM} SHIFT vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

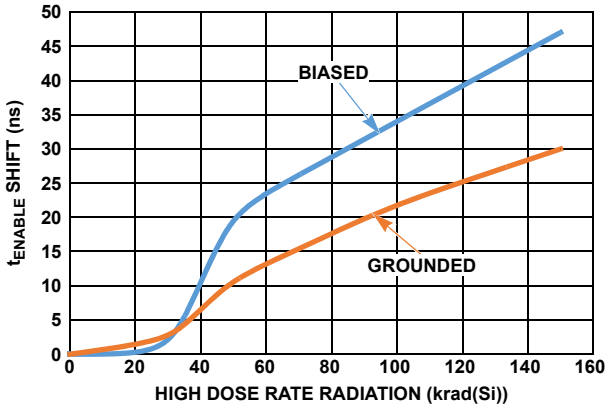


FIGURE 53. t_{ENABLE} SHIFT vs HDR RADIATION

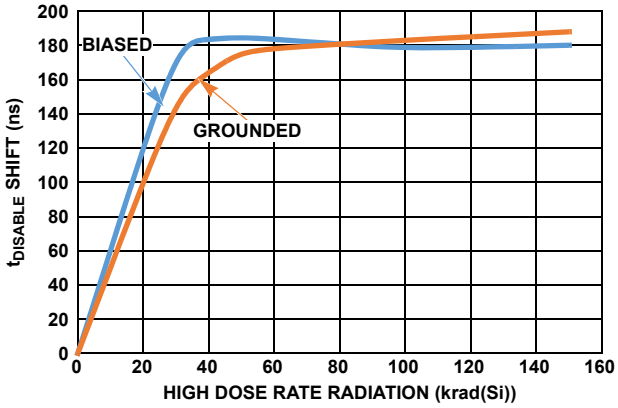


FIGURE 54. $t_{DISABLE}$ SHIFT vs HDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±15V)

Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

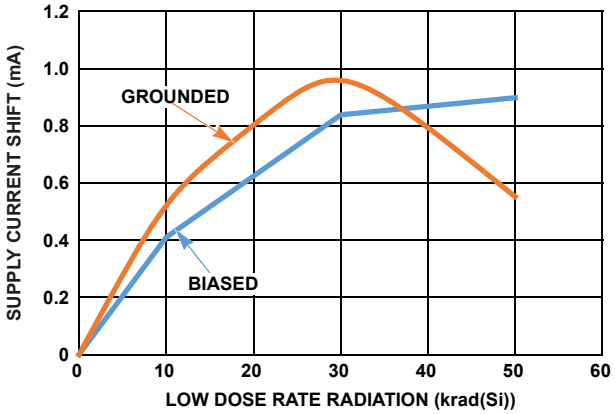


FIGURE 55. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

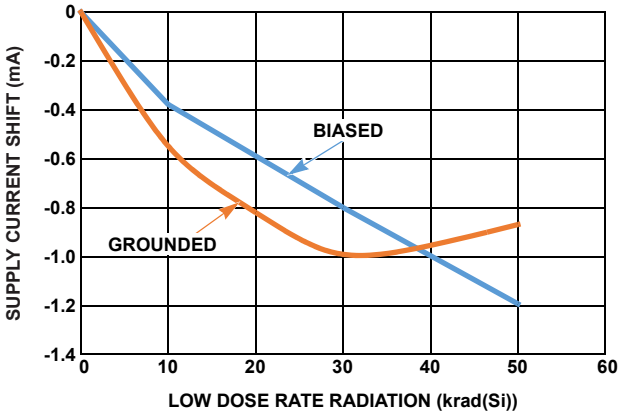


FIGURE 56. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

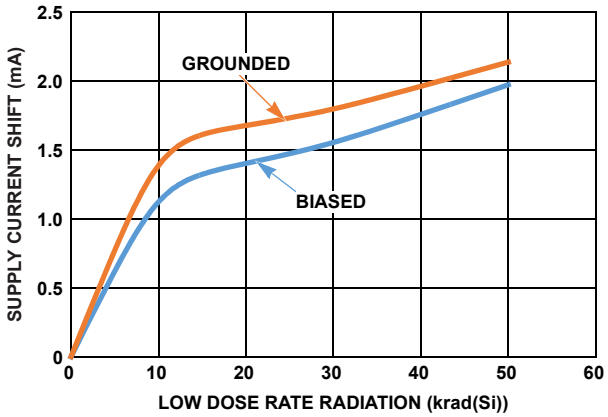


FIGURE 57. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

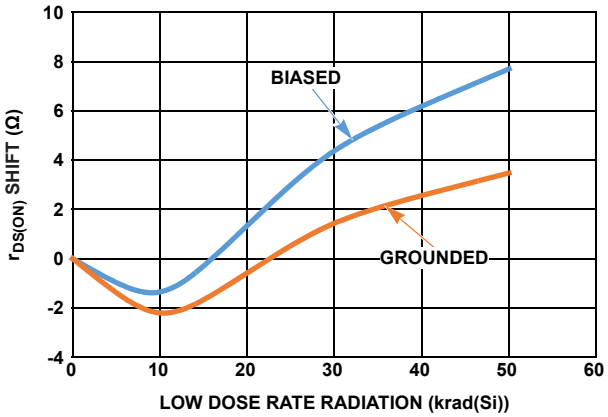


FIGURE 58. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±15V) Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

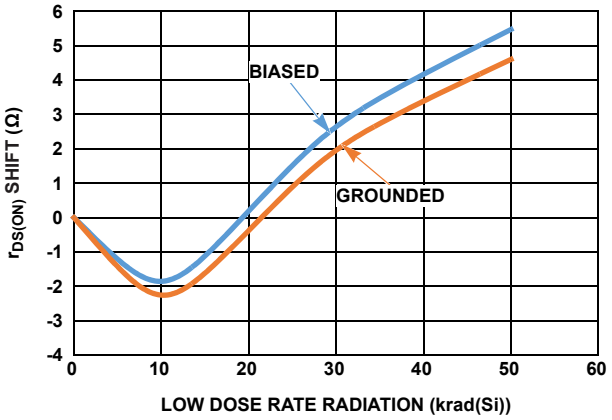


FIGURE 59. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

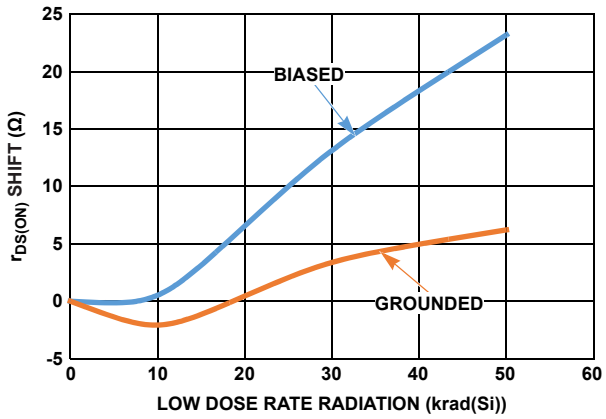


FIGURE 60. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

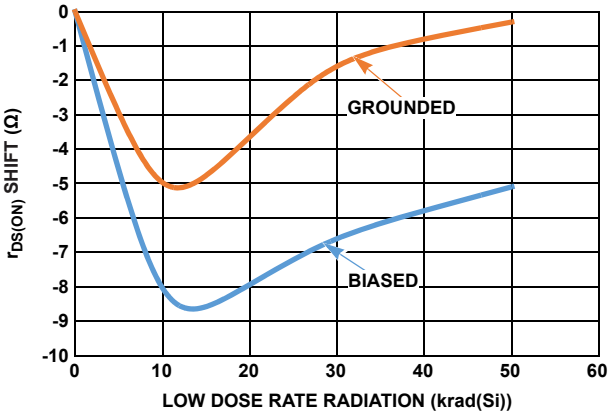


FIGURE 61. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

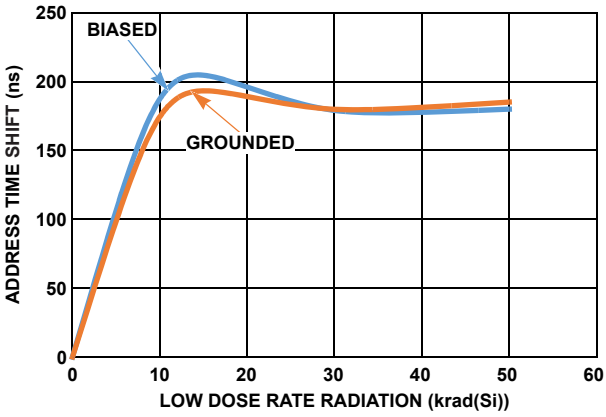


FIGURE 62. t_{ADD} SHIFT (LOW-TO-HIGH) vs LDR RADIATION

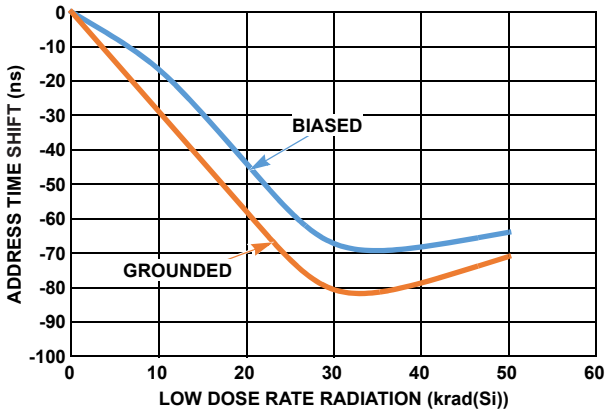


FIGURE 63. t_{ADD} SHIFT (HIGH-TO-LOW) vs LDR RADIATION

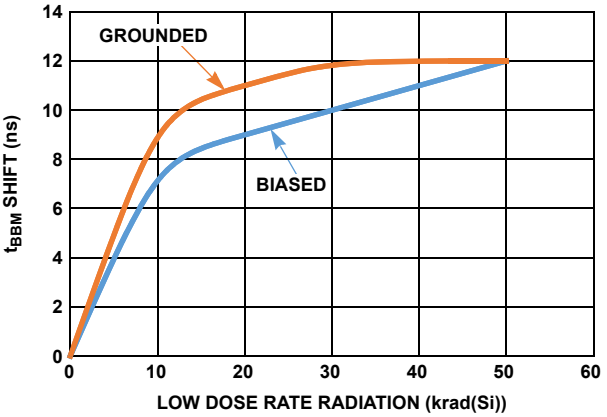


FIGURE 64. t_{BBM} SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±15V)

Unless otherwise specified, V_S = ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

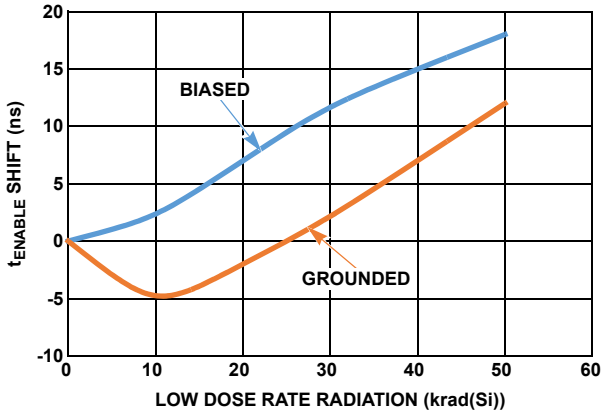


FIGURE 65. t_{ENABLE} SHIFT vs LDR RADIATION

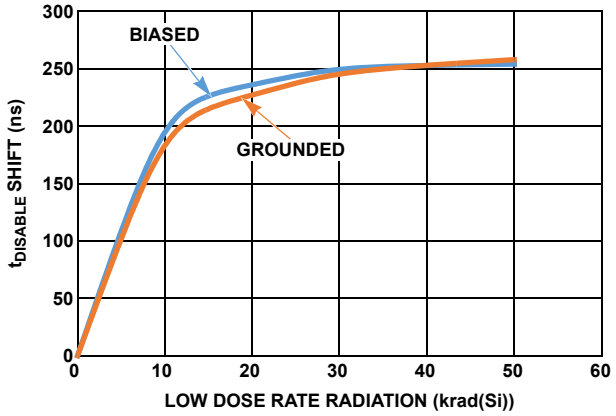


FIGURE 66. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

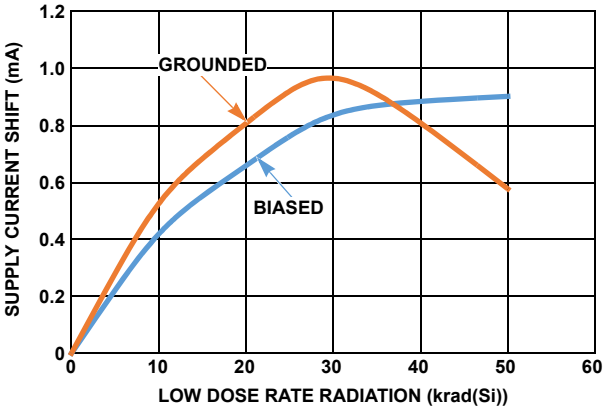


FIGURE 67. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

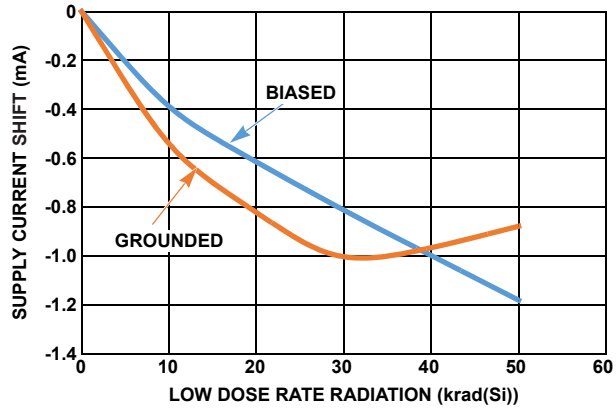


FIGURE 68. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

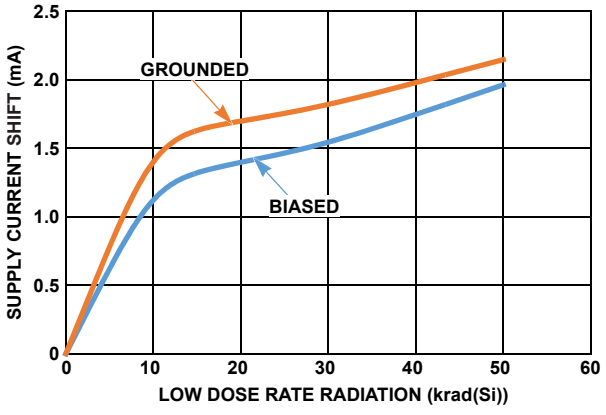


FIGURE 69. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

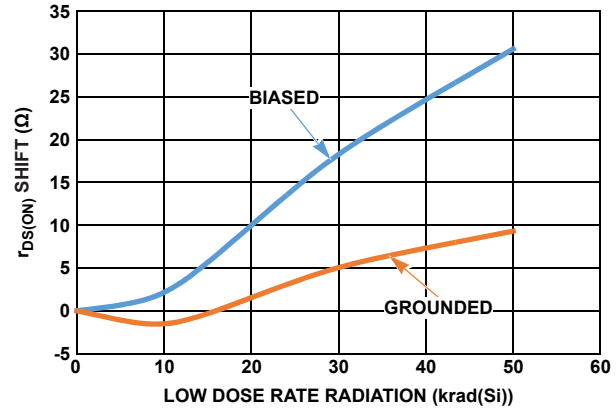


FIGURE 70. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

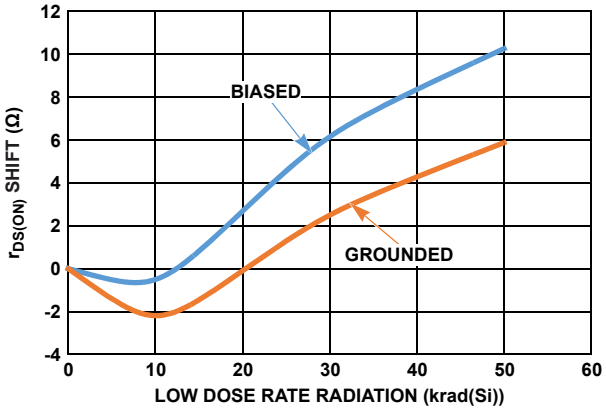


FIGURE 71. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

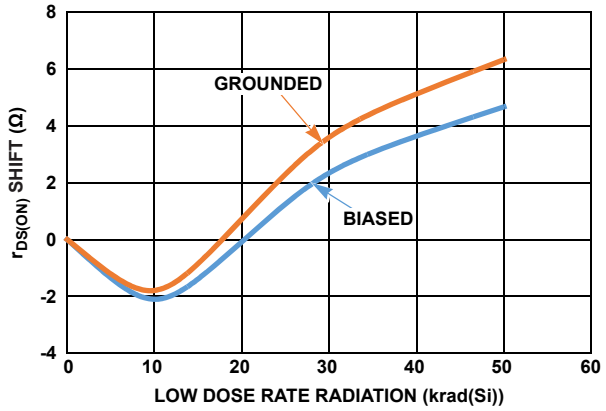


FIGURE 72. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

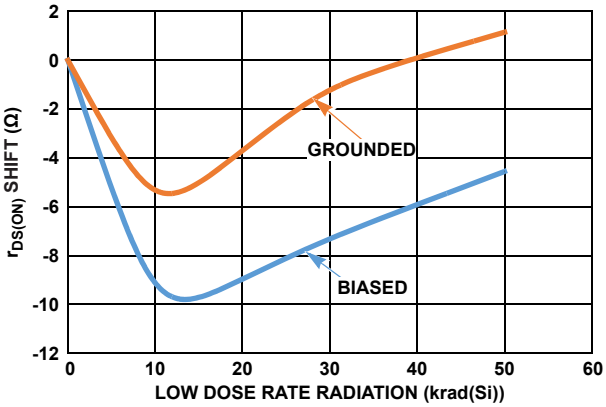


FIGURE 73. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

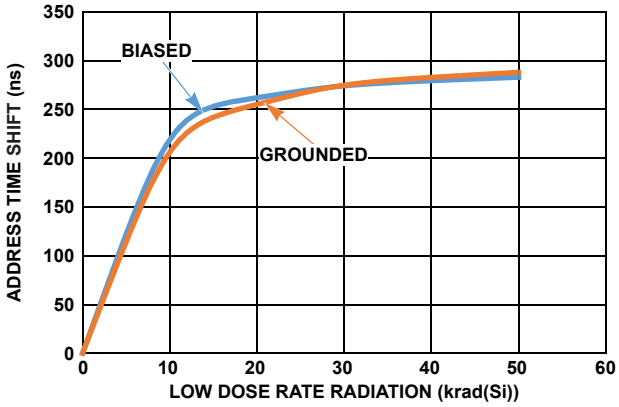


FIGURE 74. t_{ADD} SHIFT (LOW-TO-HIGH) vs LDR RADIATION

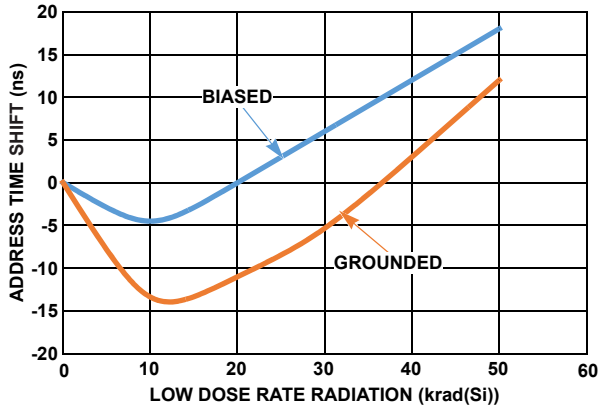


FIGURE 75. t_{ADD} SHIFT (HIGH-TO-LOW) vs LDR RADIATION

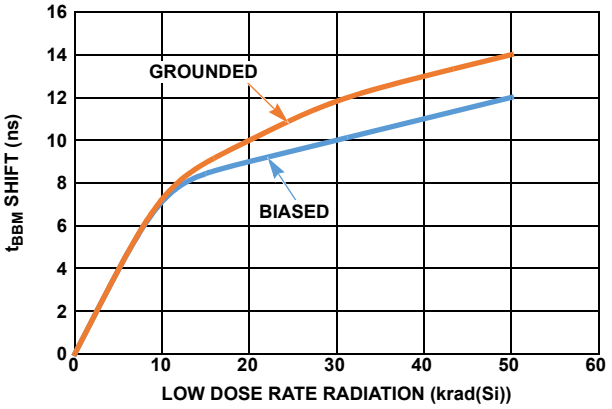


FIGURE 76. t_{BBM} SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V_S = ±12V)

Unless otherwise specified, V_S = ± 12V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

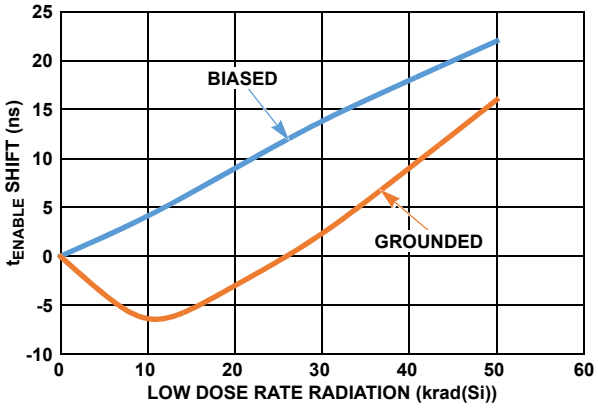


FIGURE 77. t_{ENABLE} SHIFT vs LDR RADIATION

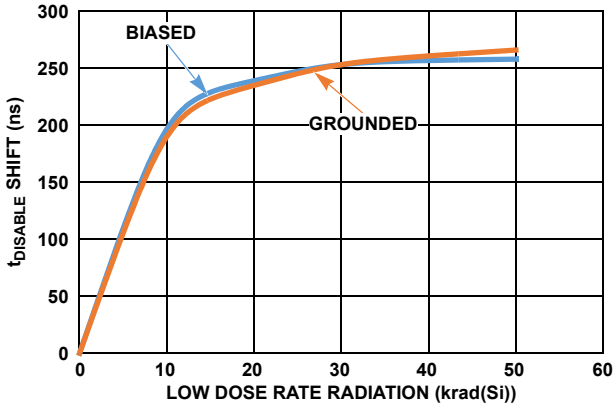


FIGURE 78. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+, V^- and VREF, however, it is recommended that all supplies power up relatively close to each other.

Overvoltage Protection

The ISL71840SEH has overvoltage protection on both the input as well as the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition (3V to 4V) past the rail), the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71840SEH. The range for VREF is between 4.5V and 5.5V with a nominal voltage of 5V. The address pins and enable are compared against roughly 30% of V_{REF} voltage (refer to Figure 79). With 5V on V_{REF}, the switching point is set to around 1.4V. This switching point allows for both 5V and 3.3V logic control.

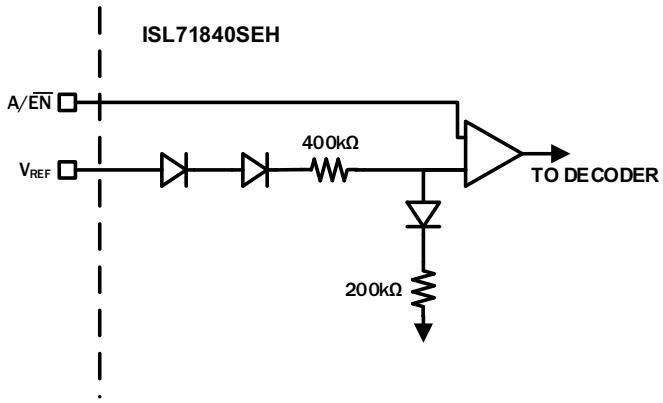


FIGURE 79. SIMPLIFIED V_{REF} CIRCUITRY

ISL71840SEH vs ISL71841SEH

There is a 32-channel version of the ISL71840SEH available in a 48 Ld CQFP. In terms of performance specs, the parts are very similar in behavior. Apart from the apparent increase in channel density, the ISL71841SEH does have slightly higher output leakage compared to the ISL71840SEH due to having more channels connected to the output. The supply current for the ISL71841SEH is also a bit higher compared to the ISL71840SEH. (See Table 1 on page 3).

Die Characteristics

Die Dimensions

2820µm x 4080µm (111mils x 161mils)
Thickness: 483µm ± 25µm (19mils ± 1mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

1.6×10^5 A/cm^2

TRANSISTOR COUNT

5682

Weight of Packaged Device

2.096 grams

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package pin 12

Metalization Mask Layout

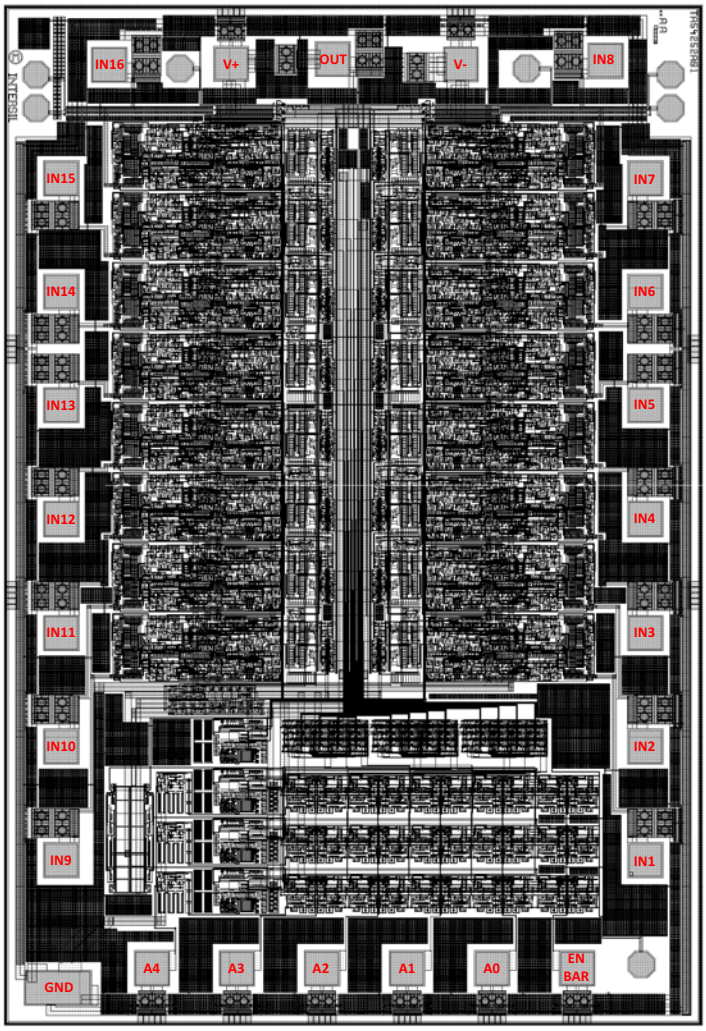


TABLE 3. ISL71840SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN8	P26	127	127	979.5	1768.5
3	V+	P27	125	125	417.5	1754.5
4	OUT	P28	125	125	-79.5	1774.5
5	V-	P1	125	125	-474.5	1756.5
7	IN16	P4	127	127	-947.5	1752.5
10	IN15	P5	127	127	-1133.5	1310.5
11	IN14	P6	127	127	-1133.5	868.5
12	IN13	P7	127	127	-1133.5	426.5
13	IN12	P8	127	127	-1133.5	-15.5
14	IN11	P9	127	127	-1133.5	-457.5
15	IN10	P10	127	127	-1133.5	-899.5
16	IN9	P11	127	127	-1133.5	-1341.5
17	GND	P12	250	125	-1147	-1839.5
18	VREF	P13	127	127	-781.5	-1763.5
19	A3	P14	127	127	-451.5	-1763.5
20	A2	P15	127	127	-121.5	-1763.5
21	A1	P16	127	127	208.5	-1763.5
22	A0	P17	127	127	538.5	-1763.5
23	EN_B	P18	127	127	868.5	-1763.5
25	IN1	P19	127	127	1133.5	-1341.5
26	IN2	P20	127	127	1133.5	-899.5
27	IN3	P21	127	127	1133.5	-457.5
28	IN4	P22	127	127	1133.5	-15.5
29	IN5	P23	127	127	1133.5	426.5
30	IN6	P24	127	127	1133.5	868.5
31	IN7	P25	127	127	1133.5	1310.5

NOTE: Origin of coordinates is the center of the die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
November 12, 2015	FN8734.1	Corrected ESD Specification references on page 5. Updated Crosstalk and Off Isolation minimum specifications on page 7. Updated VSS and VDD to V+ and V- in “Block Diagram” on page 10, “Metalization Mask Layout” on page 24 and Table 3 on page 25. Removed redundant specs from ±12V Table (V_{CTE}, V_{ISO}, V_{CT}, C_A, C_{IN}, C_{OUT}). Added Figures 26, 28 and 30. Updated Figures 33 and 45 y-axis scale. Updated Figures 31 through 78 y-axis labels. Updated top metalization thickness and composition on page 24. Updated probe coordinates table for consistency on page 25.
June 15, 2015	FN8734.0	Initial Release

About Intersil

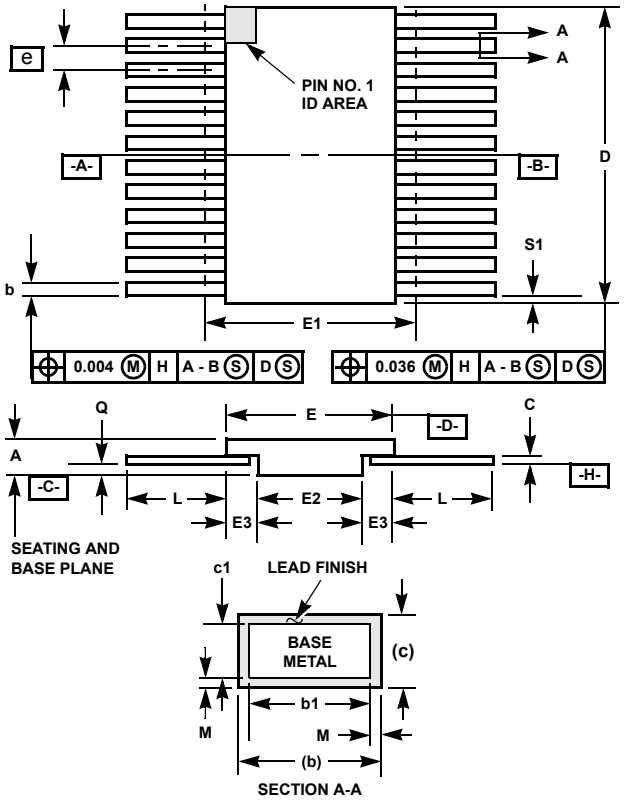
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Ceramic Metal Seal Flatpack Packages (Flatpack)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.